WHAT IS CLAIMED IS:

1.A semiconductor memory device having a gate electrode and a diffusion layer, comprising:

a plurality of memory cells each of which including the gate electrode and the diffusion layers;

a first contact layer connected to one of the diffusion layer of the memory cell;

a second contact layer connected to the first contact layer;

a bit line connected to the second contact layer; and

a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being same as a height of the first contact layer.

2. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, the first contact layer includes a W layer.

3. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, comprising the first contact layer including a first conductive film and a second conductive film.

4. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 3, the first conductive film is Ti.

5. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 3, the second conductive film is W.

6. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 1, the semiconductor memory device is one of a NAND type nonvolatile memory device and a NOR type memory device.

7. A memory card including the semiconductor memory device recited in claim 1.

8. A card holder to which the memory card recited in claim 7 is inserted.

9. A connecting device to which the memory card recited in claim 7 is inserted.

10. The connecting device according to the claim 9, the connecting device is configured to be connected to a computer.

11. A memory card including the semiconductor memory device recited in claim 1 and a controller which controls the semiconductor memory device.

12. A card holder to which the memory card recited in claim 11 is inserted.

13. A connecting device to which the memory card recited in claim 11 is inserted.

14. The connecting device according to the claim 13, the connecting device is configured to be connected to a computer.

15 An IC card on which an IC chip that includes the semiconductor memory device recited in claim 1 is located.

16.A semiconductor memory device having a gate electrode and a diffusion layer, comprising:

a plurality of memory cells each of which including the gate electrode and the diffusion layer;

an insulating film formed above side and top surfaces of the gate electrode of the semiconductor memory device;

a first interlayer insulating layer formed between the gate electrode of the semiconductor memory device;

a first contact layer formed in the first interlayer insulating layer and connected to the diffusion layer;

a second interlayer insulting layer formed on the first inter layer insulating layer ;

a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer;

a bit line connected to the second contact layer; and

a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being same as a height of the first contact layer.

17. The semiconductor memory device having a gate electrode and a diffusion layer

according to claim 1, the first contact layer includes a W layer.

18. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, a position of a top surface of the insulting film formed above the gate electrode of the semiconductor memory device is same as that of the top surface of the first interlayer insulating layer.

19. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, a position of a top surface of the insulting film formed above the gate electrode of the semiconductor memory device is different from that of the top surface of the first interlayer insulating layer.

20. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, the conductive layer is a source line.

21. The semiconductor memory device having a gate electrode and a diffusion layer according to claim 16, the semiconductor memory device is one of a NAND type nonvolatile memory device and a NOR type memory device.

22. A memory card including the semiconductor memory device recited in claim 16.

23. A card holder to which the memory card recited in claim 22 is inserted.

24. A connecting device to which the memory card recited in claim 22 is inserted.

25. The connecting device according to the claim 24, the connecting device is configured to be connected to a computer.

26. A memory card including the semiconductor memory device recited in claim16 and a controller which controls the semiconductor memory device.

27. A card holder to which the memory card recited in claim 26 is inserted.

28. A connecting device to which the memory card recited in claim 26 is inserted.

29. The connecting device according to the claim 28, the connecting device is configured

to be connected to a computer.

30 An IC card on which an IC chip that includes the semiconductor memory device recited in claim 26 1 is located.

31. A method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer, comprising:

forming a plurality of memory cells each of which including the gate electrode and the diffusion layer;

forming a first interlayer insulating film among the gate electrodes of the plurality of the memory cells;

forming a first contact hole and a second contact hole, the first contact hole reaches one of the diffusion layers of the plurality of the memory cells and the second contact hole reaches at least two of the diffusion layers of the plurality of the memory cells;

forming a first conductive layer in the first contact hole and a second conductive layer in the second contact hole;

forming a second interlayer insulating film on the first interlayer insulating film;

forming a third contact hole in the second interlayer insulating film;

forming a third conductive layer in the third contact hole, the third conductive layer connected to the first conductive layer; and

forming a bit line connected to the third conductive layer.

32. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, a height of the first conductive layers is same as that of the second conductive layer.

33. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, the forming of the first contact layer is steps of forming a first conductive film in the first contact hole, and forming a second conductive film on the first conductive film in the first contact hole.

34. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, the forming of the second contact layer is steps of a first conductive film in the first contact hole, and forming a second conductive film on the first conductive film in the first contact hole.

35. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, further comprising, forming an insulating film to cover the gate electrodes of the plurality of the memory cells after forming the plurality of memory cells.

36. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 35, the insulating film is a silicon nitride.

37. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, the forming of a first interlayer insulating film among the gate electrodes comprises steps of forming the first interlayer insulating film, and removing portion of the first interlayer insulating film so as to expose an upper surface of the insulating film that is formed to cover the gate electrode.

38. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 31, the forming of a first interlayer insulating film among the gate electrodes comprises steps of forming the first interlayer insulating film, and removing portion of the first interlayer insulating film so as to keep the first interlayer insulating film above the gate electrode.

39. A method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer, comprising:

forming a plurality of memory cells each of which including the gate electrode and the diffusion layer;

forming a first interlayer insulating film among the gate electrodes of the plurality of the memory cells;

removing portions of the first interlayer insulating film and forming a first contact hole and a second contact hole, the first contact hole reaches one of the diffusion layers of the plurality of the memory cells and the second contact hole reaches at least two of the diffusion layers of the plurality of the memory cells;

forming a first conductive layer in the first contact hole and a second conductive layer in the second contact hole;

forming a second interlayer insulating film on the first interlayer insulating film, the first conductive layer, and the second conductive layer;

removing a portion of the second interlayer insulting film and forming a third contact hole;

forming a third conductive layer in the third contact hole, the third conductive layer connected to the first conductive layer; and

forming a bit line connected to the third conductive layer.

40. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, the forming of the first contact layer is steps of forming a first conductive film in the first contact hole, and forming a second conductive film on the first conductive film in the first contact hole.

41. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, the forming of the second contact layer is steps of forming a first conductive film in the first contact hole, and forming a second conductive film on the first conductive film in the first contact hole.

42. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, further comprising, forming an insulating film to cover the gate electrodes of the plurality of the memory cells after forming the plurality of memory cells.

43. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 42, the insulating film is a silicon nitride.

44. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, the forming of a first interlayer insulating film among the gate electrodes comprises steps of forming the first interlayer insulating film, and removing portion of the first interlayer insulating film so as to expose an upper surface of the insulating film that is formed to cover the gate electrode.

45. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, the forming of a first interlayer insulating film among the gate electrodes comprises steps of forming the first interlayer insulating film, and removing portion of the first interlayer insulating film so as to keep the first interlayer insulating film above the gate electrode.

46. The method of manufacturing a semiconductor memory device having a gate electrode and a diffusion layer according to claim 39, a height of the first conductive layers is same as that of the second conductive layer.